TITLE OF THE INVENTION

A DESIGN METHOD FOR A VIDEO SIGNAL PROCESSING INTEGRATED CIRCUIT AND INTEGRATED CIRCUIT AND VIDEO SIGNAL PROCESSING APPARATUS THEREBY

CLAIM OF PRIORITY

[0001] This application makes reference to, incorporates the same herein, and claims all benefits accruing under 35 U.S.C §119 from an application entitled *A Design Method for a Video Signal Processing Integrated Circuit and Integrated Circuit and Video Signal Processing Apparatus Thereby* earlier filed in the Korean Industrial Property Office on 16 June 2000, and there duly assigned Serial No. 2000-33230 by that Office.

BACKGROUND OF THE INVENTION

Field of the Invention

[0002] The present invention relates to a video signal processing apparatus and a design method therefor, and more particularly, to a design method for a video signal processingintegrated circuit (IC), in which to solve the shortage of pin ports caused by designing a video signal processor in a

single IC, a vertical synchronization signal is output and a quasi synchronization signal is input through a single pin port, and an IC and a video signal processing apparatus thereby.

Description of the Related Art

[0003] The signal processing field in a video system can be divided into an audio signal processing field and a video signal processing field, and the video signal processing field can be divided again into a color signal processing section and a luminance signal processing section. The conventional video system is formed of separate IC chip sets for an audio signal processing unit, a color signal processing unit, a luminance signal processing unit, respectively, but in line with the recent development in the IC integration technologies, a Y/C one-chip IC, in which a color signal processing unit and a luminance signal processing unit are formed in one chip set, or an A/V one-chip, in which an audio signal processing unit, a color signal processing unit and a luminance signal processing unit are formed in one chip set, is used.

[0004] By reducing the number of signal processing ICs, the manufacturing cost for a product can be reduced and particularly, through implementation of an external discrete circuit on an IC chip set, the space on a printed circuit board (PCB) can be saved, which is advantageous in making a smaller product. Also, it is advantageous to manufacturing products when more external circuits are implemented in one IC chip together with unifying signal processing units in one chip set.

[0005] However, the unification of signal processing units in one chip and implementation of external circuits in the chip requires more ports and can cause a problem of shortage of pins in the

chip. Particularly, the number of pins in the A/V one-chip IC, which is used in the recent video apparatuses, is about 80, and reduction of the number of pins became a more important issue to product designers than integration technologies.

SUMMARY OF THE INVENTION

[0006] It is an object of the present invention to provide a design method for a video signal integrated circuit (IC), in which a vertical synchronization dividing circuit is formed inside the IC without increasing the number of IC pin ports, and a vertical synchronization signal is output through a pin port through which a quasi synchronization signal is input, and an IC and a video signal processing apparatus using the same.

[0007] To accomplish the above object of the present invention, there is provided a video signal processing integrated circuit (IC) which is used in a video recording/reproducing apparatus, the video signal processing IC having a composite synchronization dividing means for dividing a composite synchronization signal from a video signal; a vertical synchronization dividing means for dividing a vertical synchronization signal from the composite synchronization signal; a single pin port for outputting the vertical synchronization signal and inputting a quasi vertical synchronization signal; and a switching means for outputting the vertical synchronization signal, which is input from the vertical synchronization dividing means, to the pin port, or outputting the quasi vertical synchronization signal, which is input from the pin port, to the quasi vertical synchronization inserting means.

[0008] To accomplish another object of the present invention, there is also provided a video signal processing apparatus having a recording and reproducing processor for modulating/demodulating a signal to record or reproduce an input video signal; a composite synchronization dividing means for dividing a composite synchronization signal from the video signal input from the recording and reproducing processor; a single pin port for outputting the vertical synchronization signal and inputting a quasi vertical synchronization signal; a first switching means for outputting the vertical synchronization signal, which is input from the vertical synchronization dividing means, to the pin port, or outputting the quasi vertical synchronization signal, which is input from the pin port, to a quasi vertical synchronization inserting means; the quasi vertical synchronization inserting means for inserting the quasi vertical synchronization signal, which is input from the first switching means, to a video signal, which is processed for reproducing signal; and a second switching means for outputting a signal, which is input from the output terminal of the quasi vertical synchronization inserting means, to a video output port in a special reproducing mode, and outputting a signal, which is applied to the input terminal of the quasi synchronization inserting means, to the video output port in any of the remaining modes.

[0009] To accomplish another object of the present invention, there is also provided a method for designing a video signal processing IC having a recording and reproducing processor for modulating/demodulating a signal, a vertical synchronization dividing means, and a quasi vertical synchronization inserting means, the method having the steps of forming a pin port for outputting a vertical synchronization signal and a pin port for inputting a quasi vertical synchronization signal in a single pin port; and designing the pin port to operate as an input port for inputting a quasi

vertical synchronization signal, which is output from a microprocessor located separate from the video signal processing IC, in a reproducing mode, and to operate as an output port for outputting a vertical synchronization signal, which is divided in the vertical synchronization dividing means, to the microprocessor separate from the video signal processing IC, in the remaining modes.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] A more complete appreciation of the present invention, and many of the attendant advantages thereof, will become readily apparent as the same becomes better understood by reference to the following detailed description when considered in conjunction with the accompanying drawings in which like reference symbols indicate the same or similar components, wherein:

[0011] FIG. 1 illustrates an exemplary video signal processing system illustrating a background problem which the present invention is intended to overcome; and

[0012] FIG. 2 illustrates a video signal processing system according to the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0013] Hereinafter, embodiments of the present invention will be described in detail with reference to the attached drawings. The present invention is not restricted to the following embodiments, and many variations are possible within the spirit and scope of the present invention. The embodiments of the present invention are provided in order to more completely explain the

present invention to anyone skilled in the art.

[0014] FIG. 1 illustrates an exemplary video signal processing system in which a vertical synchronization dividing circuit 30 is implemented as a discrete circuit separate from a video signal processor 20.

[0015] The video signal processor 20 is formed of one chip having a recording/reproducing processor 21, a quasi vertical synchronization inserting unit 22, and a composite synchronization signal dividing unit 23.

[0016] The recording/reproducing processor 21, in a recording mode, modulates an input video signal (Video In) and provides the modulated signal to a deck unit 10 so that the signal can be recorded in a recording medium, and in a reproducing mode, demodulates a signal read by a video head of the deck unit 10, and outputs the signal in the form of a video signal before recording.

[0017] A composite synchronization signal dividing unit 23 receives a video signal output from the recording/reproducing processor 21, and separates the composite synchronization signal (C-Sync), containing a vertical synchronization signal and a horizontal synchronization signal, from the video signal.

[0018] A vertical synchronization dividing unit 30 located separate from the video signal processor 20 separates the vertical synchronization signal (V-Sync) from the composite synchronization signal output from the composite synchronization signal dividing unit 23. The composite synchronization signal (C-Sync) and the vertical synchronization signal (V-Sync) are theninput to a microprocessor 40.

[0019] Microprocessor 40, in a recording mode, controls a drum motor and a capstan motor contained in the deck 10, using the composite synchronization signal and vertical synchronization signal as servo control signals. Microprocessor 40 also generates a quasi vertical synchronization signal (QV, Quasi V-Sync) in special reproducing modes such as a still mode or a slow mode. Here, the quasi vertical synchronization signal QV is a vertical synchronization signal which is arbitrarily generated using a head switching pulse (not shown) for switching a video head contained in the deck 10.

[0020] A quasi vertical synchronization inserting unit 22 receives a quasi vertical synchronization signal (QV) output from the microprocessor 40, and inserts the QV into a video signal received from the recording/reproducing processor 21 during one of the special reproducing modes.

[0021] In the video signal processing system, formed as described above, if the vertical synchronization dividing unit 30, which is located separate from the video signal processor 20 in FIG. 1, is formed inside, or as an integral part of, the video signal processor 20, an additional IC pin port for outputting a vertical synchronization signal should be prepared. Therefore, the number of IC pin ports increases.

[0022] As shown in FIG. 2, a signal processing system to which the present invention is applied has a deck unit 10, a video signal processor 50, and a microprocessor 60.

[0023] Here, the video signal processor 50 IC is formed of a recording/reproducing processor 51, a composite synchronization signal dividing unit 53, a vertical synchronization signal dividing unit 53, a quasi vertical synchronization inserting unit 54, a switching unit 57, a switching unit 55, and

a single pin port 56 for outputting a vertical synchronization signal and inputting a quasi vertical synchronization signal.

[0024] For impedance matching, resistors 61 and 62 are connected to a port for inputting a vertical synchronization signal and a port for outputting a quasi vertical synchronization signal, respectively, of the microprocessor 60, and the microprocessor 60 is connected to the pin port 56 of the video signal processor 50 through the resistors 61 and 62.

[0025] The recording/reproducing processor 51, in a recording mode, modulates an input video signal (Video In), and transmits the modulated signal to the deck unit 10 so that the signal can be recorded in a recording medium, and, in a reproducing mode, demodulates a signal read by the video head of the deck unit 10, and outputs the signal in the form of a video signal before recording.

[0026] The composite synchronization signal dividing unit 53 receives a video signal output from the recording/reproducing processor 51, and separates a composite synchronization signal (C-Sync), containing a vertical synchronization signal and a horizontal synchronization signal, from the video signal. Then, the composite synchronization signal (C-Sync) is input to the microprocessor 60.

[0027] The vertical synchronization dividing unit 53 of the video signal processor 50 separates a vertical synchronization signal (V-Sync) from the composite synchronization signal (C-Sync) output from the composite synchronization signal dividing unit 52.

[0028] In a recording mode, the microprocessor 60 controls the drum motor and capstan motor contained in the deck 10 using the composite synchronization signal and vertical synchronization signal as servo control signals.

[0029] Microprocessor 60 generates a quasi vertical synchronization signal (QV, Quasi V-Sync) in special reproducing modes such as a still mote or a slow mode. Here, the quasi vertical synchronization signal is a vertical synchronization signal which is arbitrarily generated using a head switching pulse (not shown) for switching a video head contained in the deck 10.

[0030] The quasi vertical synchronization inserting unit 54 receives the quasi vertical synchronization signal (QV) output from the microprocessor 60, and inserts the quasi vertical synchronization signal (QV) into the video signal output from the recording/reproducing processor 51 during a special reproducing mode.

[0031] The switching unit 55 controls connections so that a video output port is connected to an output terminal of the quasi vertical synchronization inserting unit 54 in a special reproducing mode (SPB), and is connected to an output terminal of the recording/reproducing processor 51 in the remaining modes ($\overline{SPB}$). Though the quasi vertical synchronization inserting unit 54 and the switching unit 55 are separately formed in the embodiment of FIG. 2, a circuit for the switching unit 55 can be designed to be included in the quasi vertical synchronization inserting unit 54 so that a quasi vertical synchronization signal can be inserted into an output video signal only in a special reproducing mode.

[0032] The switching unit 57 is connected to an output terminal of the vertical synchronization dividing unit 53 and an input terminal of the quasi vertical synchronization inserting unit 54, and also connected to the pin port 56 operating as an input/output port. Here, the switching unit 57 controls connections so that the pin port 56 is connected to the quasi vertical synchronization inserting unit

54 in a special reproducing mode (PB), and connected to the vertical synchronization dividing unit 53 in the remaining modes ($\overline{PB}$).

[0033] Accordingly, since the pin port 56 of the video signal processor 50 is used as an output port for a vertical synchronization signal in a mode other than a special reproducing mode, and is used as an input port for a quasi vertical synchronization signal in a special reproducing mode, the pin port 56 is connected to the microprocessor 60 through resistors 61 and 62 for impedance matching. Also, for safer impedance matching, the input port for a vertical synchronization (V-Sync) signal of the microprocessor 60 is designed to have a high impedance state during a special reproducing mode, and the output port of a quasi synchronization (QV) signal is designed to operate as an output port in the special reproducing mode, and to have a high impedance state in a recording mode.

[0034] According to this method for designing a video IC and a video signal processing apparatus, the vertical synchronization signal output port and the quasi vertical synchronization input port can be formed in a signal pin port 56 of an IC, and therefore a vertical synchronization dividing circuit can be designed inside a video signal processing IC without increasing the number of IC pin ports.

[0035] By designing a vertical synchronization dividing circuit inside an IC without increasing the number of pins in a video signal processing IC, the present invention can reduce the number of components, material costs, and save the PCB space. In addition, by integrating the vertical synchronization dividing circuit inside an IC, the component difference of a discrete device can be reduced, which enhances IC performance.